Electro-VLSI 2023

19th - 20th Oct, 2023 (Hybrid Mode)

VIT BHOPAL

Hosted by VLSI Research Group
School of Electrical and Electronics Engineering
VIT Bhopal University

GUEST SPEAKER

Dr. Vishal Sharma

PhD, SoC Design Engineer at Intel Technology

THE SPEAKERS

- **Dr. Beohar, *Sr. Member IEEE* from VIT Bhopal is an IIT Indore alumnus, is renowned for his groundbreaking work in Low-power Nanoscale Device, Memory Circuit Design, boasting over 35 publications in eminent platforms like IEEE and Springer.**
- **Dr. Sarkar from VIT Bhopal, is a MS from Ryerson Univ, Torronto and a PhD from Jadavpur Univ. She is a recognized authority in Digital VLSI, VHDL, ASIC and has publications in reputed SCI Journals. Her research area is Design Space Exploration.**
- **Dr. Upadhyay is with VIT Bhopal and is a PhD from IIT BHU. His special focus lies on nanoelectronics. He had worked as a research assistant at NUS Singapore and has made notable contributions in the domain of thin-film nanotechnology-based optoelectronic devices.**
- **Ms. Sonal Gupta is a faculty in VIT Bhopal. She has done her B.E (Hons.) from PEC,Chandigarh and a M.Tech from IIT Bombay. She has a rich industrial experience at Texas Instruments, India in Embedded Controller group. Currently, as a Ph.D. Scholar at IIT Delhi, her research gravitates towards the intricate facets of system connectivity.**

Dr. Ankur Beohar

Dr. Pallabi Sarkar

Dr. Deep Upadhyay

Ms. Sonal Gupta

IEEE STUDENT BRANCH VIT BHOPAL

intel

Talk Highlights: Electro-VLSI-2023

- **Dr. Ankur Beohar**

  Topic: Devices to Circuits

  - Dive into low Power Nanoscale Devices.
  - Explore circuit applications & gate structures.

- **Dr. Deep Chandra Upadhyay**

  Topic: Nanostructures in Sensors

  - Learn about nanostructures.
  - Discover their use in high-performance photodetectors.

- **Dr. Pallabi Sarkar**

  Topic: Optimization in ASIC Design

  - Deep dive into Digital System Design optimization.
  - Focus on Architectural Level Synthesis for ASIC Design.

- **Ms. Sonal Gupta**

  Topic: VLSI Systems via Vivado

  - Get hands-on with an application-based approach.

- **Dr. Vishal Sharma**

  Hands-On Session: Analog VLSI Methodologies

  - Hands on experiece on Analog VLSI Design.
  - Schematic design, simulation and analysis.
  - Efficient Layout design(with DRC & LVS check) using Cadence Virtuoso.

Exclusively curated for B.Tech, M.Tech, M.E., PhD scholar and faculty from Electronics, Electrical, Instrumentation, & Computer Science.

Participate in hands-on workshops, acquainting you with advanced VLSI tools.

-Early Bird registration: Just Rs. 250/- per person.

Organizer

Dr. DEBASHIS ADHIKARI

Dean, SEEE

VIT Bhopal University

Registration fee Details

For all participants : *250/-*
Last date of Registration: 10th October

Account Details (for NEFT payments)

Account Holder: VIT SEEE CLUB
Account No.: 7107689443
IFSC Code: IDIB000V143
Branch Code: 02953
Bank Name: INDIAN BANK

Registration Link (Please register after completion of payment)

https://forms.gle/wAUpYPxhZWNKNzRB9

Important Dates

Last date for registration: 10th October
Confirmation to the participants: 11th October

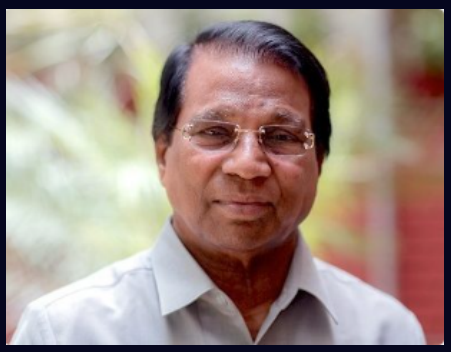
E-Certification

Participants will receive an e-certificate when they attend the session.

About the university

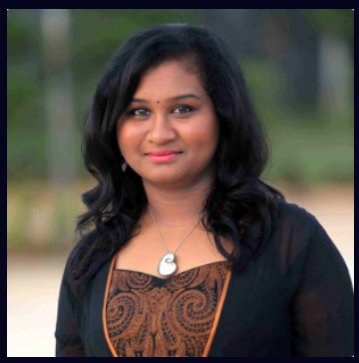
VIT Bhopal University was established in 2017 with a global perspective which is dedicated to make leaders of future generations. The university is led by Dr G. Viswanathan, Founder and Chancellore, Mr. Sankar Viswanathan, vice president Ms. kadhambari S. Viswanathan, Assistant Vice President. It is lush green campus of 260 acres situated at the heart of India, between the two cleanest cities, indore and Bhopal. Within a short span of time VIT Bhopal University has become one of the best chosen university by the students for its future ready courses such B.Tech in Aerospace Enginnering, Artificial Intelligence and Machine Learning, Cyber Security and Digital Fornsics, Bio engineering etc. VIT Global Outlook will empower its aspirant to attain excellence through learning. The Comprehensive Teaching methodology designed by the University i.e. Collaborative and Active Learning Through Technology (CALTech) pedagogy adopted by all 100% doctoral faculties. It redefines the approach to learning, education and building knowledge-based societies in the country. Collarboration with reputed national and international organizations and strategic partnership with universities around the world are established, to prepare globally competent generation of professionals. Currently there are 10000+ students enrolled in more than 15 programs from 26 states across India.

Leadership



Dr. G. VISWANATHAN
Chancellor

Mr. SANKAR VISWANATHAN
Vice President



Ms. KADHAMBARI S. VISWANATHAN
Asst. Vice President

Dr. SENTHIL KUMAR ARUMUGAM
Vice - Chancellor (i/c)

Dr. PRADYUMNA YADAV
Registrar